

Yuanlong Li

Ph.D. Candidate

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RESEARCH INTERESTS

I am broadly interested in systems and cross-stack research problems in modern, large-scale datacenters. More specifically, my current research focuses on designing novel hardware-software interfaces for virtual memory and Function-as-a-Service (FaaS) systems through hardware-software co-design.

EDUCATION

- **École Polytechnique Fédérale de Lausanne (EPFL)** 09/2020 - Present
 - Doctor of Philosophy in Computer Science
 - Advisor: Prof. Babak Falsafi
- **Harbin Institute of Technology (HIT)** 09/2014 - 07/2016
 - Master of Science in Particle and Nuclear Physics
 - Advisor: Prof. Jingbo Zhang
- **Harbin Institute of Technology (HIT)** 09/2010 - 07/2014
 - Bachelor of Engineering in Electronics Engineering
 - Advisor: Prof. Fangfa Fu

PUBLICATION

- **Single-Address-Space FaaS with Jord** ISCA'25
 - Rearchitecting FaaS with a single-address-space design
 - Y. Li, A. Bhattacharyya, M. Kumar, A. Bhattacharjee, Y. Etsion, B. Falsafi, S. Kashyap, and M. Payer
- **Imprecise Store Exceptions** ISCA'23
 - Handling exceptions generated by logic embedded in the cache/memory hierarchy
 - Y. Li*, S. Gupta*, Q. Kang, A. Bhattacharjee, B. Falsafi, Y. Oh, and M. Payer
- **SecureCells: A Secure Compartmentalized Architecture** IEEE S&P'23
 - Compartmentalization with ns-scale operations using hardware support
 - A. Bhattacharyya, F. Hofhammer, Y. Li, S. Gupta, A. Sanchez, B. Falsafi, and M. Payer
- **SystolicAttention: Fusing FlashAttention within a Single Systolic Array** arXiv
 - Enhancing systolic array architecture for reduction operations in FlashAttention
 - J. Lin, Y. Li, G. Chen, and T. Bourgeat
- **QFlex 3.0: Fast and Accurate ARM Server Simulation** AGPC'25
 - The next version of QFlex simulator with sampling methodology
 - S. Lin, A. Ansari, A. Chakraborty, B. Eryilmaz, Y. Li, M. Alian, and B. Falsafi
- **Rethinking IOMMU for Future IO Devices** YArch'25
 - Eliminating address translation overheads from IO
 - M. Kumar, Y. Li, Y. Etsion, A. Bhattacharjee, A. Basu, B. Falsafi, S. Kashyap, and M. Payer

AWARDS

- **EPFL EDIC fellowship** 2020
- **Graduate First-class Academic Scholarship** 2015
- **National Encouragement Scholarship** 2013
- **National Encouragement Scholarship** 2011

WORK EXPERIENCE

- **SiFive China, Inc.** 02/2020 - 09/2020
 - Senior Engineer
 - Designer of Load/Store Unit (LSU) and L2 cache controller (L2C) of SiFive China's first server CPU
- **Arm China, Inc.** 05/2019 - 01/2020
 - Engineer
 - Designer of the cryptographic co-processor for ARMv8-M CPUs
- **Unisoc, Inc.** 07/2016 - 05/2019
 - Advanced Senior ASIC Design Engineer
 - Designer of L1/L2 TLBs of Unisoc's second CPU
 - Full-system verification and post-silicon validation of Unisoc's CPUs

TEACHING EXPERIENCE

- **Parallelism and Concurrency in Software (CS-302)** 2024
 - Teaching Assistant under Prof. Arkaprava Basu and Prof. Babak Falsafi
- **Introduction to Multiprocessor Architecture (CS-307)** 2022, 2023
 - Teaching Assistant under Prof. Babak Falsafi
- **Computer Architecture (CS-200)** 2024
 - Teaching Assistant under Prof. Paolo Ienne

PROJECTS

- **Midgard**
 - <https://github.com/goshuh/midgard>
 - Hardware implementation of Midgard/Jord
- **Midgard on OpenXiangShan**
 - https://github.com/goshuh/midgard_xiangshan
 - Integration of Midgard/Jord and OpenXiangShan
- **Midgard Linux**
 - https://github.com/parsa-epfl/midgard_linux
 - Linux port of Midgard/Jord
- **XiangShan over FireSim**
 - <https://github.com/parsa-epfl/xsofs>
 - Running OpenXiangShan over FireSim
- **SecureCells on RocketChip**
 - <https://github.com/HexHive/seccell-rocket>
 - Hardware implementation of SecureCells on RocketChip
- **QFlex**
 - <https://github.com/parsa-epfl/qflex>
 - A family of quick, accurate, and flexible simulators of multi-node computer systems built on QEMU/Flexus